Miller Capacitance Cancellation to Improve SiC MOSFET's Performance in a Phase-Leg Configuration

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***Abstract*—The drain to gate capacitance (Miller capacitance) of SiC MOSFETs leads to the Miller effect during switching transients. The Miller capacitance in a phase-leg configuration causes the crosstalk, the interaction between the two complementary switches, and the Miller plateau during the switching transient. The Miller effect reduces the switching speed, reduces reliability, and increases electromagnetic interference. In this article, by injecting a mirror cancellation current, the effects of Miller capacitance are canceled. The proposed technique includes a two-stage sensing and injection network to compensate for the nonlinearity of the Miller capacitance. The proposed technique can suppress both positive and negative gate voltage spikes induced by the crosstalk and reduce the switching power loss with the increased switching speed. Because no external control signals are required in the proposed technique, it can work with almost all commercial gate drivers. The detailed design for this proposed technique is presented in this article. The proposed technique was validated with both simulations and experiments.**

***Index Terms*—Crosstalk, electromagnetic interference (EMI), Miller capacitance, Miller effect, Miller plateau, SiC MOSFET.**

I. Introduction

SiC mosfets have smaller ON-resistance, smaller junction capacitance [1], and higher maximum operating temperature than Si devices at similar power ratings. As a result, SiC MOSFET is a promising candidate to replace Si insulated-gate bipolar transistor (IGBT) in high power applications, such as electric vehicles and the aviation industry. However, the high-speed potential of SiC MOSFETs has not been fully utilized in these applications. One of the major barriers is the Miller effect. For the SiC MOSFETs in a phase-leg configuration, the Miller effect influences the switching performance of SiC MOSFETs through two couplings: the coupling between power loop and drive loop [3], and the coupling between the top and bottom switches.

The coupling between the power loop and the drive loop causes the gate voltage to be clamped at a relatively constant value for a period of time during the switching transient. This period of time is also known as the Miller plateau [2]. The Miller plateau impacts the switching speed of the device. The coupling between the top and bottom switches is the interactions between the two switches in a phase-leg configuration at high *dv/dt* switching [3]. The positive and negative voltage spikes are induced at the gates of the devices; this is also known as the crosstalk effect. The positive voltage spike causes potential false triggering, which leads to hazardous shoot-through failure. The negative gate voltage spike could cause the gate–oxide breakdown [4]. In industrial applications, both false triggering and negative voltage over-range must be avoided by all means.

The common-source inductance (CSI) [3] also contributes to the crosstalk effect. Reducing the CSI with package optimization techniques, such as the Kelvin connection, can mitigate the crosstalk caused by the CSI. In contrast, the Miller capacitance is an intrinsic property of the semiconductor devices. Reducing the crosstalk caused by the Miller capacitance is a major challenge.

The existing research has proposed techniques to address either the crosstalk or the Miller plateau. For the crosstalk suppression, the proposed techniques mainly fall into three categories.

1) Reducing the Switching Speed: Increasing the value of the gate resistor or adding an external gate capacitor effectively mitigate the crosstalk [5], [6] at the cost of a lower speed.
2) Control the Gate Loop Impedance: The induced gate voltage is a function of the drive loop impedance. The low-impedance path between the gate and source of the victim device can mitigate the crosstalk [7]–[9]. In [10], a high gate drive loop impedance is also proposed to damp the gate voltage oscillation, while the Miller capacitance is precharged and predischarged to avoid crosstalk. Controlling the gate drive loop impedance usually requires complicated assistive circuits and control logic.
3) Applying Multilevel Gate Voltage [11]–[15]: Multilevel gate voltage techniques do not suppress the induced gate voltage spikes. Instead, different levels of gate voltage are added to the gate during the OFF-state to prevent false triggering and negative voltage over-range after the crosstalk has occurred. In the cases of SiC MOSFETs, since both positive- and negative-induced gate voltage spikes are high due to high switching speed, the OFF-state gate voltage must be controlled precisely to avoid both false triggering and negative breakdown. The design of a multilevel gate driver becomes costly and challenging.

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TABLE I
COMPARISON OF THE EXISTING CROSSTALK SUPPRESSION TECHNIQUES AND THE PROPOSED TECHNIQUE

Literatures	PERFORMANCE				Crosstalk Suppression Technique Category	
	Positive spike suppressed by	Negative spike suppressed by	Increased switching speed	Additional control		
[4]	2.5%	30%	No	No	Passive	Gate impedance control
[7] (TO-247)	66%	0%	Yes	No	Passive	Gate impedance control
[8] [9]	N/A	50%	Yes	Yes	Active	Gate impedance control
[10]	50%	67%	No	Yes	Active	Gate impedance control
[12]	N/A	0%	No	Yes	Active	Shifting gate voltage levels
[13]	N/A	80%	No	No	Active	Shifting gate voltage levels
[18] [19]	N/A	N/A	Yes	Yes	Active	Closed-loop gate drive
This paper	80%	90%	Yes	No	Active	Miller cap cancellation

Some research attempts to reduce the Miller plateau. The closed-loop driving techniques were proposed in [16]–[19]. These closed-loop driving techniques control the gate voltage/current based on the difference between the sampled waveforms and the desired waveforms. The closed-loop techniques require many additional analog and digital circuits. The crosstalk is not suppressed in these closed-loop driving techniques. In some cases, applying closed-loop driving increases the chances of false triggering [18] and requires additional circuits [19].

In this article, a Miller effect suppression technique is proposed. Different from the previous research, the proposed technique focuses on the root cause of the Miller effect, so both crosstalk and the Miller plateau can be greatly suppressed. With the proposed technique, the nonlinear Miller capacitance can be equivalently canceled. Requiring no external control strategies, the proposed technique can work with most commercial drivers or be integrated inside the power module package. A thorough comparison between the existing and the proposed techniques is summarized in Table I. In Table I, the data are based on the experimental results in the cited articles. If the technique uses the gate voltage shifting techniques, the gate voltage spikes are not essentially suppressed, so it is not applicable (N/A) in Table I. From Table I, the proposed technique reduces the gate voltage spikes and increases the switching speed much more than the existing techniques. The rest of the article will be organized as follows. The Miller effect during the switching transient is analyzed in Section II. Based on the analysis, the Miller capacitance cancellation technique (MCCT) is proposed in Section III. The working principle is analyzed. Section IV discusses the design of the proposed technique. In Section V, simulations and experiments are conducted to validate the proposed technique. Finally, Section VI concludes this article.

II. MILLER EFFECT ANALYSIS DURING THE SWITCHING TRANSIENTS OF SiC MOSFETS

The switches in a phase-leg circuit have four switching states: top switch turn-ON transient, top switch turn-OFF transient, bottom switch turn-ON transient, and bottom switch turn-OFF transient. During the switching transients of one switch, the other switch is OFF. Because the switching transient analysis has been presented in other articles [2], [20], [24], this section only focuses on the role of the Miller capacitance.

The four switching transients of the devices in a phase-leg configuration are shown in Fig. 1. The currents flowing through the junction capacitances of the M are shown in Fig. 1. Because the top and bottom switches are symmetrical, the transient analysis of M_1 is the same as M.

During M_1's turn-ON transient in Fig. 1(a) and (e), the gate driver's voltage rises to V_H, the drain to source voltage V_{ds} of the M rises drastically, and V_{gs1} reaches the Miller plateau in Fig. 1(e). Because of the high dV_{ds}/dt, a Miller current flowing through the Miller capacitance C_{gd} of M is induced. The drain to gate voltage V_{dg} of M is given by

$$V_{dg} = V_{ds} - V_{gs}. \tag{1}$$

The Miller current is given by

$$i_{\text{Miller}} = C_{gd}\left(\frac{dV_{ds}}{dt} - \frac{dV_{gs}}{dt}\right). \tag{2}$$

The Miller current flowing through the gate resistor R_g and gate to source capacitance C_{gs} meet

$$\frac{V_{gs} - V_L}{R_g} + C_{gs}\frac{dV_{gs}}{dt} = i_{\text{Miller}}. \tag{3}$$

V_{gs} can be solved with (2) and (3)

$$V_{gs} = R_g C_{gd}\frac{dV_{ds}}{dt}\left(1 - e^{-\frac{1}{R_g C_{iss}}t}\right) - e^{-\frac{1}{R_g C_{iss}}t}\int R_g C_{gd}\frac{d^2V_{ds}}{dt^2}e^{\frac{1}{R_g C_{iss}}t}dt + V_L \tag{4}$$

where $C_{iss} = C_{gs} + C_{gd}$.

In (4), in most of the existing pieces of literature [2], [3], [8], [9], V_{ds} is modeled as a trapezoidal waveform; so, $\frac{d^2V_{ds}}{dt^2} = 0$. Equation (4) reduces to

$$V_{gs} = R_g C_{gd}\frac{dV_{ds}}{dt}\left(1 - e^{-\frac{1}{R_g C_{iss}}t}\right) + V_L. \tag{5}$$

Equation (5) has a similar expression to the existing research [8], [9]. Equation (5) gives a quick estimation of the induced gate voltage. Because $\frac{dV_{ds}}{dt}$ is positive in this state, the induced gate voltage is higher than the gate driver's OFF-state voltage V_L. In actual SiC MOSFET applications, $\frac{dV_{ds}}{dt}$ is not constant as in Fig. 1(e); therefore, (4) is more accurate than (5).

Similarly, during M_1's turn-OFF transient in Fig. 1(b) and (e), the drain to source voltage V_{ds} of M drops drastically and V_{gs1} reaches the Miller plateau in Fig. 1(e). V_{gs} has the same expression as (4) except dV_{ds}/dt is negative. This indicates that the induced gate voltage is lower than V_L.

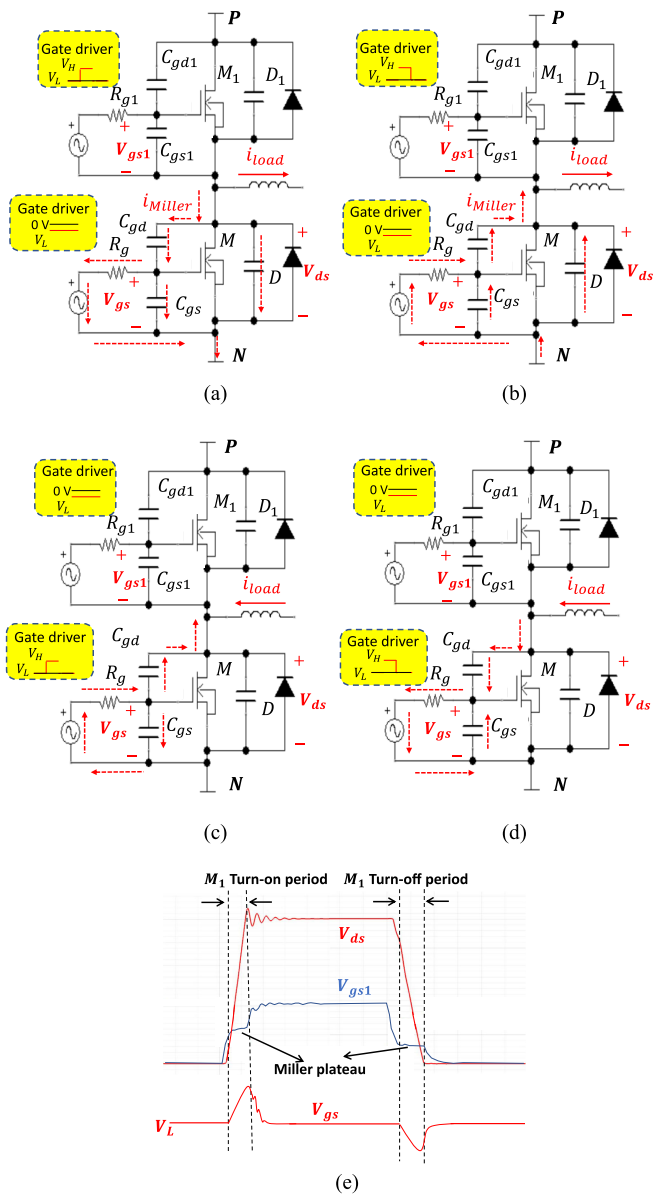


Fig. 1. Switching transients of devices in a phase-leg configuration. (a) M_1's turn-ON transient, M is OFF. (b) M_1's turn-OFF transient, M is OFF. (c) M's turn-ON transient, M_1 is OFF. (d) M's turn-OFF transient, M_1 is OFF. (e) Waveforms.

During the M's turn-ON transient in Fig. 1(c) (the time-domain waveform is not shown here), the gate driver's voltage rises to V_H. The driving current i_g is given by

$$i_g = \frac{V_H - V_{gs}}{R_g} = C_{gd}\left(\frac{dV_{gs}}{dt} - \frac{dV_{ds}}{dt}\right) + C_{gs}\frac{dV_{gs}}{dt}. \quad (6)$$

The drain to source voltage V_{ds} of M decreases and V_{gs} reaches the Miller plateau, which makes $dV_{gs}/dt \approx 0$. Equation (6) can be simplified as

$$\frac{V_H - V_{gs}}{R_g} = -C_{gd}\frac{dV_{ds}}{dt}. \quad (7)$$

The turn-ON switching speed is, therefore, given by

$$\frac{dV_{ds}}{dt}\Big|_{\text{on}} = -\frac{V_H - V_{gs}}{C_{gd}R_g}. \quad (8)$$

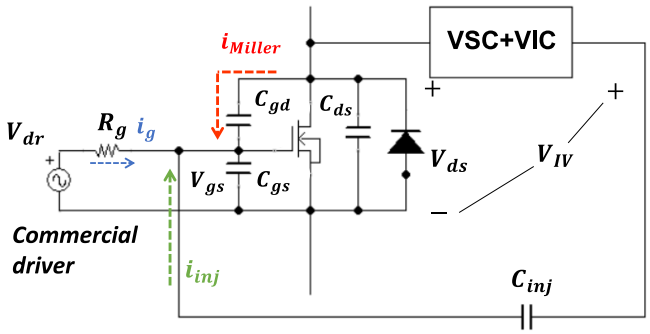


Fig. 2. SiC MOSFET with the Miller capacitance cancellation.

Similarly, during the M's turn-OFF transient in Fig. 1(d) (the time-domain waveform is not shown here), the drain to source voltage V_{ds} of M increases and V_{gs} reaches the Miller plateau. The turn-OFF speed of M is given by

$$\frac{dV_{ds}}{dt}\Big|_{\text{off}} = \frac{V_{gs} - V_L}{C_{gd}R_g}. \quad (9)$$

V_{gs} in (8) and (9) is the gate to source voltage at the Miller plateau, which is determined by the load current [20].

From (2) to (9), the root cause of the crosstalk and the Miller plateau is the Miller capacitance C_{gd}. If $C_{gd} = 0$, both the Miller plateau and the crosstalk would be eliminated.

III. MCCT and Its Working Principle

A. Principle of Miller Capacitance Cancellation

The Miller capacitance can be equivalently canceled by injecting a mirror current i_{inj} with the same magnitude but inverse phase as the Miller current i_{Miller} to the gate of the SiC MOSFET. Fig. 2 shows the concept. The compensation circuit includes the voltage sensing circuit (VSC) and the voltage inverting circuit (VIC). VSC and VIC sense V_{ds} and generate inject voltage V_{IV}. V_{IV} is added to the injection capacitor C_{inj} to generate injection current i_{inj}. The condition of cancellation is $i_{\text{inj}} = -i_{\text{Miller}}$.

The Miller capacitance C_{gd} is nonlinear as a function of V_{ds}, but the injection capacitance C_{inj} is constant; therefore, the voltage gain of the compensation circuit VSC+VIC should be adjusted based on V_{ds} to approximately compensate the nonlinearity of C_{gd}. A higher V_{ds} corresponds to a smaller C_{gd}; therefore, a smaller gain is needed. A lower V_{ds} corresponds to a bigger C_{gd}; therefore, a bigger gain is needed. To achieve this, the gain can be adjusted in two stages or multistages based on the magnitude of the sensed V_{ds}. A two-stage solution will be presented in this article.

B. Circuit Realization

Fig. 3 shows the proposed MCCT that comprises VSC, VIC, and C_{inj}.

1) VSC Analysis: The VSC in Fig. 4 consists of a voltage-dividing impedance network and a low-power MOSFET Q_1. $Z_5 = \frac{1}{sC_5}$ represents the impedance of the drain to source junction capacitance C_5 of Q_1. Z_2 and Z_3 represent the impedances of the capacitances, which are the total of an external capacitor and

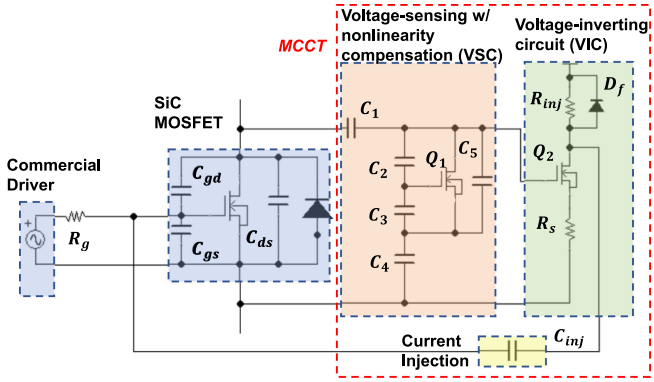


Fig. 3. MCCT applied to a SiC MOSFET.

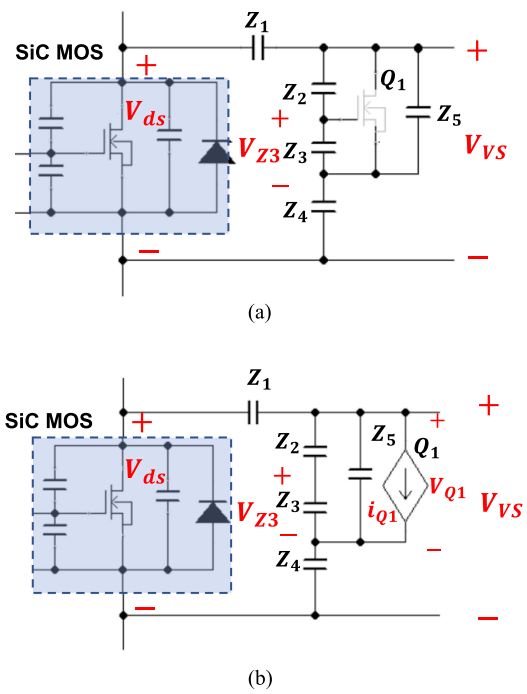


Fig. 4. VSC with two gains. (a) Stage 1. (b) Stage 2.

the junction capacitance of Q_1, between the gate and the drain and between the gate and the source. The input voltage of the VSC is the drain to source voltage V_{ds} of the SiC MOSFET. To cancel the nonlinear Miller capacitance, which is a function of V_{ds}, of the SiC MOSFET, the VSC operates in two stages with two different gains at different V_{ds}.

a) Stage 1: $V_{ds}<V_{dsth}$: In Fig. 4, the gate to source voltage V_{Z3} of Q_1 is determined by the capacitance network. At stage 1, V_{Z3} is smaller than Q_1's threshold voltage V_{thQ1}, which is corresponding to an SiC MOSFET's drain to source voltage V_{dsth}, Q_1 is OFF, as shown in Fig. 4(a). Because the input impedance of VIC is much larger than the output impedance of VSC (will be proved later), the VIC's loading effect on the output voltage V_{VS} can be ignored. The dynamic gain G_{vs1} of VSC is given by

$$G_{vs1} = \frac{dV_{VS}/dt}{dV_{ds}/dt} = \frac{Z_{Q1}+Z_4}{Z_{VD}+Z_{Q1}} \tag{10}$$

where

$$Z_{Q1} = \frac{Z_5\left(Z_2+Z_3\right)}{Z_2+Z_3+Z_5} \tag{11}$$

$$Z_{VD} = Z_1 + Z_4. \tag{12}$$

The V_{dsth} is given by

$$V_{dsth} = V_{thQ1}\frac{\left(Z_{Q1}+Z_{VD}\right)\left(Z_2+Z_3\right)}{Z_{Q1}Z_3}. \tag{13}$$

The output impedance Z_{Vo1} of VSC at stage 1 is

$$Z_{Vo1} = \left(Z_{Q1} + Z_4\right)//Z_1. \tag{14}$$

b) Stage 2: $V_{ds}\geq V_{dsth}$: When V_{ds} is higher than V_{dsth}, Q_1 conducts current i_{Q1} in the saturation region, as shown in Fig. 4(b). The current bypasses C_2 and C_3 and C_5 via the small channel resistance of Q_1. The channel current i_{Q1} is given by

$$i_{Q1} = g_{mQ1}\cdot\left(V_{Z3}-V_{thQ1}\right) \tag{15}$$

where g_{mQ1} is the transconductance of Q_1. Solving the drain to source voltage V_{Q1} of Q_1 from Fig. 4(b)

$$V_{Q1} = \frac{V_{ds}+g_{mQ1}Z_{VD}V_{thQ1}}{1+\frac{Z_{VD}}{Z_{Q1}}+\frac{g_{mQ1}Z_3Z_{VD}}{Z_2+Z_3}}. \tag{16}$$

In the design, Z_{VD} should be big enough at switching frequencies to reduce the leakage current flowing from the SiC MOSFET's drain to source. As a result, in the design, $|g_{mQ1}Z_{VD}|>10^7$. On the other hand, $|1+\frac{Z_{VD}}{Z_{Q1}}|$is designed as <100. The $V_{ds}$of the SiC MOSFET is limited by the maximum operating voltage. Therefore, the following conditions can be met:

$$\left|\frac{g_{mQ1}Z_3Z_{VD}}{Z_2+Z_3}\right| \gg \left|1+\frac{Z_{VD}}{Z_{Q1}}\right| \tag{17}$$

$$\left|g_{mQ1}Z_{VD}V_{thQ1}\right| \gg \left|V_{ds}\right|. \tag{18}$$

Based on (17) and (18), the V_{Q1} in (16) can be simplified as

$$V_{Q1} = V_{thQ1}\frac{Z_2+Z_3}{Z_3}. \tag{19}$$

The output voltage of VSC at stage 2 is, therefore

$$V_{VS} = \frac{Z_4}{Z_{VD}}\left(V_{ds}-V_{Q1}\right)+V_{Q1}. \tag{20}$$

Since $V_{Q1}$is constant in (19) and the input impedance of VIC is much larger than the output impedance of VSC (will be proved later), the dynamic gain G_{vs2} of VSC at stage 2 is

$$G_{vs2} = \frac{dV_{VS}/dt}{dV_{ds}/dt} = \frac{Z_4}{Z_{VD}}. \tag{21}$$

Because of (19), Q_1 can be replaced with a constant voltage source in ac analysis. The output impedance Z_{Vo2} of VSC at stage 2 is, therefore, given by

$$Z_{Vo2} = Z_1//Z_4. \tag{22}$$

Based on (10) and (21), by adjusting the impedance Z_1–Z_4, the VSC will have two gains at different V_{ds}. G_{vs1} is a large gain when V_{ds} is low and G_{vs2} is a small gain when V_{ds} is high.

In the VSC, the junction capacitance changes nonlinearly with V_{Q1}. It is worth discussing the impact of the Q_1's junction capacitance on the performance of the VSC. In stage 1, V_{Q1} changes from 0 V to $(V_{thQ1}\frac{Z_2+Z_3}{Z_3})$. In this range, based on

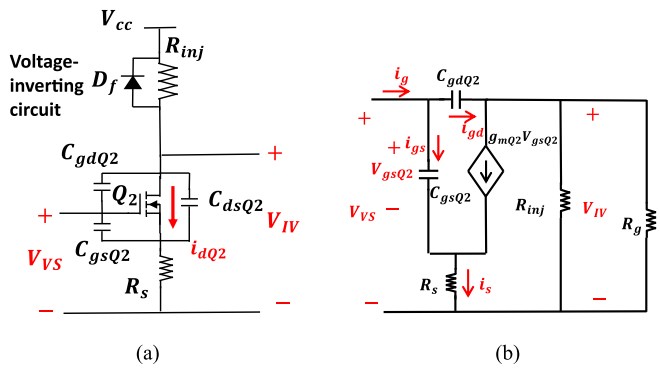


Fig. 5. (a) VIC. (b) Small-signal model.

the datasheet, G_{vs1} changes only 6% due to the nonlinearity of the junction capacitance. In stage 2, V_{Q1} is clamped to a constant value given by (19). Therefore, the value of the junction capacitance does not change. The gain G_{vs2} is constant. In general, the nonlinearity of Q_1's junction capacitance has an ignorable impact on the performance of the VSC. As a result, in rest of this article, the value of Z_2, Z_3, and Z_5 are considered constant during the analysis and design.

2) VIC Analysis: The VIC is to invert the output voltage V_{VS} of the VSC in Fig. 5(a). The VIC consists of two resistors R_{inj} and R_s, a low-power MOSFET Q_2, and a diode D_f. The VIC is powered by a DC power supply V_{cc}, which can be the same power supply used by the SiC MOSFET's gate driver. D_f clamps V_{IV}–V_{cc} and protect Q_2 when there is current flowing from C_{inj}. R_{inj} is the injection resistor. R_s is the negative feedback resistor to improve VIC's temperature stability [25], increase VIC's input impedance Z_{in} and set the saturation operating point of Q_2.

When V_{VS} is higher than the threshold voltage V_{thQ2} of Q_2, Q_2 operates in the saturation region, and the channel current i_{dQ2} is

$$i_{dQ2} = g_{mQ2}\ (V_{gsQ2} - V_{thQ2}) \tag{23}$$

$$V_{gsQ2} = V_{VS}\ - R_s i_{dQ2}. \tag{24}$$

Solving (23) and (24) for i_{dQ2}

$$i_{dQ2} = \frac{g_{mQ2}\,(V_{VS} - V_{thQ2})}{1 + g_{mQ2}R_s}. \tag{25}$$

In Fig. 3, R_g is the gate resistor of the SiC MOSFET. Based on the circuit theory, in the frequency range 2–100 MHz, the impedance of C_{inj} (6.8 nF) is much smaller than R_{inj} (10 Ω) and R_g (15 Ω), and the impedances of C_{gd} (100 pF) and C_{gs} (170 pF) are much bigger than R_{inj} and R_g; the output voltage V_{IV} of the VIC is, therefore

$$V_{\text{IV}} = V_{cc}\ - i_{dQ2}R_g//R_{\text{inj}}. \tag{26}$$

Substituting (25) into (26) yields

$$V_{\text{IV}} = V_{cc}\ - \frac{g_{mQ2}R_g//R_{\text{inj}}\,(V_{VS} - V_{thQ2})}{1 + g_{mQ2}R_s}. \tag{27}$$

The dynamic gain G_{vi} of VIC is, therefore

$$G_{vi} = \frac{dV_{\text{IV}}}{dt}\Big/\frac{dV_{VS}}{dt} = -\frac{g_{mQ2}R_g//R_{\text{inj}}}{1 + g_{mQ2}R_s}. \tag{28}$$

If $R_L = R_g//R_{\text{inj}}$, the input impedance Z_{in} of VIC is solved based on the small-signal model in Fig. 5(b) as

$$Z_{\text{in}} = \left(\frac{1}{1 + A_1}\right)\left(R_s + \frac{g_{mQ2}R_s + 1}{sC_{gsQ2}}\right) \tag{29}$$

where $A_1 = (\frac{C_{gdQ2}}{C_{gsQ2}})\cdot(\frac{(sC_{gsQ2}R_S + g_{mQ2}R_s + 1)(g_{mQ2}(R_L + R_s) + 1)}{1 + g_{mQ2}R_s})$.

Based on (14), (22), (29), the circuit parameters, and the parameters of Q_1 and Q_2 (IRLMS1503) at the operating point, $g_m \approx 2$ S, $R_s = 7.5\ \Omega$, $C_{gsQ2} \approx 175$ pF, $C1 = 8.2$ pF, $C2 \approx 400$ pF, $C3 \approx 475$ pF, $C4 = 1$ nF, and $C5 \approx 150$ pF, it is found that $Z_{\text{in}} >> Z_{Vo1}$, Z_{Vo2}, and VIC's loading effect on G_{vs1} and G_{vs2} is ignored.

3) Current Injection to Cancel Miller Plateau and Crosstalk: From (10), (21), and (28), the total voltage gain G_{MCCT} is

$$G_{\text{MCCT}} = \frac{dV_{\text{IV}}/dt}{dV_{ds}/dt} = \begin{cases} G_{vs1}G_{vi} = -\frac{Z_{Q1} + Z_4}{Z_{VD} + Z_{Q1}}\cdot\frac{g_{mQ2}R_g//R_{\text{inj}}}{1 + g_{mQ2}R_s}, & V_{ds} < V_{dsth} \\ & \text{(stage 1)} \\ G_{vs2}G_{vi} = -\frac{Z_4}{Z_{VD}}\cdot\frac{g_{mQ2}R_g//R_{\text{inj}}}{1 + g_{mQ2}R_s}, & V_{ds} \geq V_{dsth} \\ & \text{(stage 2)}. \end{cases} \tag{30}$$

When V_{ds} of the SiC MOSFET changes drastically, the cancelation current i_{inj} will be injected to the gate of the SiC MOSFET through the injection capacitor C_{inj}, as shown in Fig. 2. i_{inj} is given by

$$i_{\text{inj}} = C_{\text{inj}}\left(\frac{dV_{\text{IV}}}{dt} - \frac{dV_{gs}}{dt}\right) = C_{\text{inj}}\,G_{\text{MCCT}}\frac{dV_{ds}}{dt} - C_{\text{inj}}\frac{dV_{gs}}{dt}. \tag{31}$$

During the turn-ON transient of the complementary switch, V_{ds} rises. The V_{gs} spike can be induced by the Miller current. At the same time, in Fig. 2, i_{inj} is injected. The total current flows through R_g and C_{gs} is given by

$$\frac{V_{gs} - V_L}{R_g} + C_{gs}\frac{dV_{gs}}{dt} = i_{\text{Miller}}\ + i_{\text{inj}}. \tag{32}$$

Substitute (2) and (31) into (32)

$$\frac{V_{gs-V_L}}{R_g} + C_{iss1}\frac{dV_{gs}}{dt} = (C_{gd} + C_{\text{inj}}G_{\text{MCCT}})\frac{dV_{ds}}{dt} \tag{33}$$

where $C_{iss1} = C_{gs}\ + C_{\text{inj}} + C_{gd}$.

V_{gs} can be calculated as

$$V_{gs} = R_g\ (C_{gd} + C_{\text{inj}}G_{\text{MCCT}})\frac{dV_{ds}}{dt}\left(1 - e^{-\frac{1}{R_gC_{iss1}}t}\right) - e^{-\frac{1}{R_gC_{iss1}}t}\int R_g\,(C_{gd} + C_{\text{inj}}G_{\text{MCCT}})\frac{d^2V_{ds}}{dt^2}e^{\frac{1}{R_gC_{iss1}}t}dt + V_L. \tag{34}$$

In (34), when the following condition is met:

$$C_{\text{inj}} = -\frac{C_{gd}}{G_{\text{MCCT}}} \tag{35}$$

the first two terms become zero. The Miller capacitance is equivalently canceled and $V_{gs} = V_L$. The induced positive gate voltage spike is, thus, canceled.

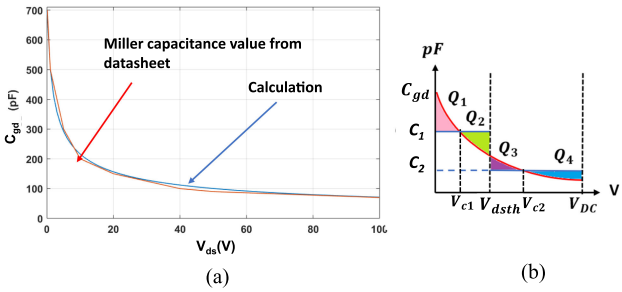


Fig. 6. C_{gd} of an SiC MOSFET SCT3060AR. (a) Comparison of the datasheet and calculation. (b) Charge equivalence with two constant capacitances.

Similarly, during the turn-OFF transient of the complimentary switch, the induced negative V_{gs} spike is also canceled when (35) is met.

During the turn-ON transient of the SiC MOSFET, the driver voltage $V_{dr} = V_H$. The gate current satisfies

$$i_g = \frac{V_H - V_{gs}}{R_g} = -\left(i_{\text{Miller}} + i_{\text{inj}}\right). \tag{36}$$

The switching speed of the SiC MOSFET is solved by substituting (2) and (31) into (36)

$$\frac{dV_{ds}}{dt}\Big|_{\text{on}} = -\frac{(V_H - V_{gs})/R_g}{(C_{gd} + C_{\text{inj}} G_{\text{MCCT}})}. \tag{37}$$

Similarly, during the device turn-OFF transient, the driver voltage $V_{dr} = V_L$, and the switching speed is given by

$$\frac{dV_{ds}}{dt}\Big|_{\text{off}} = \frac{(V_{gs} - V_L)/R_g}{(C_{gd} + C_{\text{inj}} G_{\text{MCCT}})}. \tag{38}$$

From (8), (9), (37), and (38), when (35) is met, the Miller plateau is canceled and the switching speed greatly increases.

Based on the analysis in this section, the proposed MCCT can cancel the effect of Miller capacitance. As a result, the crosstalk and Miller plateau can be canceled.

IV. Design Techniques for the Proposed MCCT

This section discusses the design for MCCT, including the compensation of the nonlinearity of the Miller capacitance, the high-frequency performance of the VSC, and the operation region of VIC and the power loss.

A. Compensating the Nonlinearity of the Miller Capacitance

It is well known that Miller capacitance C_{gd} is a function of V_{ds}. In Fig. 6(a), C_{gd} decreases quickly as V_{ds} increases. The relationship between C_{gd} and V_{ds} is given by [21]

$$C_{gd}\ (V_{ds}) = \frac{C_0}{\sqrt{1 + V_{ds}/V_0}} \tag{39}$$

where C_0 and V_0 are the dimension-related constants, and they can be acquired from datasheets. For the SiC MOSFET SCT3060AR, $C_0 = 700$ pF and $V_0 = 1.05$ V. The calculation based on (39) matches the datasheet very well in Fig. 6(a).

Because of the nonlinearity of C_{gd}, G_{MCCT} needs to be adjusted based on V_{ds} to satisfy (35) with a constant C_{inj}. In this article, two constant capacitances C_1 and C_2 are selected to equivalently represent the nonlinear C_{gd} in terms of charge. During the switching transient, the total charge transferred through the voltage dependent C_{gd} over time is equal to the total charge transferred through the two selected constant capacitances C_1 and C_2 at different V_{ds} over time, as shown in Fig. 6(b). Under such equivalence, C_{gd} is represented by

$$\begin{cases} C_1,\ V_{ds} < V_{dsth} \\ C_2,\ V_{ds} > V_{dsth}. \end{cases} \tag{40}$$

To meet (35), the gain of VSC should be designed as

$$G_{\text{MCCT}} = \begin{cases} G_{vs1} = \frac{C_1}{C_{\text{inj}}},\ V_{ds} < V_{dsth} \\ G_{vs2} = \frac{C_2}{C_{\text{inj}}},\ V_{ds} > V_{dsth}. \end{cases} \tag{41}$$

From (41), the two gains of the VSC need to meet

$$\frac{G_{vs1}}{G_{vs2}} = \frac{C_1}{C_2}. \tag{42}$$

Because the total charge flowing through C_1 and C_2 should be equal to the charge flowing through C_{gd} when V_{ds} increases from 0 V to V_{DC}, C_1 and C_2 should meet

$$\int_0^{V_{dsth}} C_1 dv_{ds} = \int_0^{V_{dsth}} C_{gd}\left(v_{ds}\right) dv_{ds} \tag{43}$$

$$\int_{V_{dsth}}^{V_{\text{DC}}} C_2 dv_{ds} = \int_{dsth}^{V_{\text{DC}}} C_{gd}\left(v_{ds}\right) dv_{ds}. \tag{44}$$

During switching transients, in Fig. 6(b), (35) is satisfied perfectly when V_{ds} is at V_{c1} and V_{c2}. When V_{ds} changes from 0 V to V_{DC}, the cancellation performance depends on the difference between the constant capacitors, namely C_1 and C_2, and the Miller capacitance. To maximize the cancellation performance, the charge difference must be minimized. Fig. 6(b) shows the charge difference Q_1–Q_4 when V_{ds} changes from 0 V to V_{DC}. Q_1–Q_4 are given by

$$Q_1 = \int_0^{V_{c1}} C_{gd}\left(v_{ds}\right) dv_{ds} - \int_0^{V_{c1}} C_1\left(v_{ds}\right) dv_{ds} \tag{45}$$

$$Q_2 = \int_{V_{c1}}^{V_{dsth}} C_1\left(v_{ds}\right) dv_{ds} - \int_{V_{c1}}^{V_{dsth}} C_{gd}\left(v_{ds}\right) dv_{ds} \tag{46}$$

$$Q_3 = \int_{V_{dsth}}^{V_{c2}} C_{gd}\left(v_{ds}\right) dv_{ds} - \int_{V_{dsth}}^{V_{c2}} C_2\left(v_{ds}\right) dv_{ds} \tag{47}$$

$$Q_4 = \int_{V_{c2}}^{V_{\text{DC}}} C_2\left(v_{ds}\right) dv_{ds} - \int_{V_{c2}}^{V_{\text{DC}}} C_{gd}\left(v_{ds}\right) dv_{ds}. \tag{48}$$

From (43) and (44), C_1 and C_2 are given by

$$C_1 = \frac{2C_0V_0\left(\sqrt{1 + \frac{V_{dsth}}{V_0}} - 1\right)}{V_{dsth}} \tag{49}$$

$$C_2 = \frac{2C_0V_0\left(\sqrt{1 + \frac{V_{DC}}{V_0}} - \sqrt{1 + \frac{V_{dsth}}{V_0}}\right)}{V_{\text{DC}} - V_{dsth}}. \tag{50}$$

Solving (45)–(50) simultaneously

$$Q_1 = Q_2 = 2C_0\,V_0 \cdot \left(\sqrt{\left(1 + \frac{V_{dsth}}{V_0}\right)} - 1\right) - C_1 \cdot V_{c1} \tag{51}$$

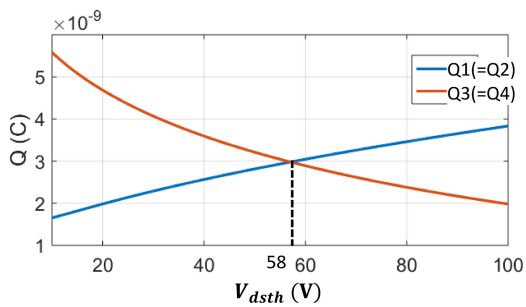


Fig. 7. Comparison of charge difference as a function of V_{dsth}.

$$Q_3 = Q_4 = 2C_0\, V_0 \cdot \left(\sqrt{\left(1+\frac{V_{c2}}{V_0}\right)} - \sqrt{\left(1+\frac{V_{dsth}}{V_0}\right)}\right) - C_2 \cdot (V_{c2} - V_{dsth}) \tag{52}$$

where

$$V_{c1} = \left(V_0\left(\frac{C_0}{C_1}\right)^2 - 1\right) \tag{53}$$

$$V_{c2} = \left(V_0\left(\frac{C_0}{C_2}\right)^2 - 1\right). \tag{54}$$

From (51) to (53), Q_1 and Q_3 are the functions of V_{dsth}, as shown in Fig. 7. To minimize the charge differences so as to minimize the crosstalk and the Miller plateau, V_{dsth} should be selected so that the bigger one of Q_1 and Q_3 is the minimum. When V_{dsth} increases from 0 V to V_{DC}, Q_1 increases and Q_3 decreases; this condition leads to $Q_1 = Q_3$, i.e., V_{dsth} should be the crossover voltage of Q_1 and Q_3 curves. It is 58 V for this case.

From (10), (21), and (42), the impedances meet

$$\frac{Z_{VD}\,(Z_{Q1}+Z_4)}{Z_4\,(Z_{VD}+Z_{Q1})} = \frac{C_1}{C_2}. \tag{55}$$

From (30) and (35), at stage 1, the capacitance of the injection capacitor is calculated by

$$C_{\mathrm{inj}} = -\frac{C_1}{G_{vs1}\cdot\frac{g_{mQ2}R_g//R_{\mathrm{inj}}}{1+g_{mQ2}R_s}}. \tag{56}$$

The value of the injection capacitor is the same at stage 2 when it is calculated from C_2 and G_{vs2} because of (42).

B. Improving the High-Frequency Performance of the MCCT

In Section III, when $V_{ds}>V_{dsth}$ at stage 2, because conditions (17) and (18) are met, the dynamic gain of VSC is given by (21). However, because impedance Z_{VD} is inversely proportional to frequencies, the terms on the left side of the inequality in (17) and (18) decrease at a slope −20 dB/dec as the frequency increases. As a result, at high frequencies, (17) and (18) are not well met and G_{vs2} will not be equal to (21). The cancellation condition (35) will not be met, so the Miller current cannot be well canceled.

To improve MCCT's high-frequency performance, conditions (17) and (18) should hold at high frequencies, for example, at least ten times of $1/t_{sw}$, where t_{sw} is the smaller one of the rising and falling time of V_{ds}.

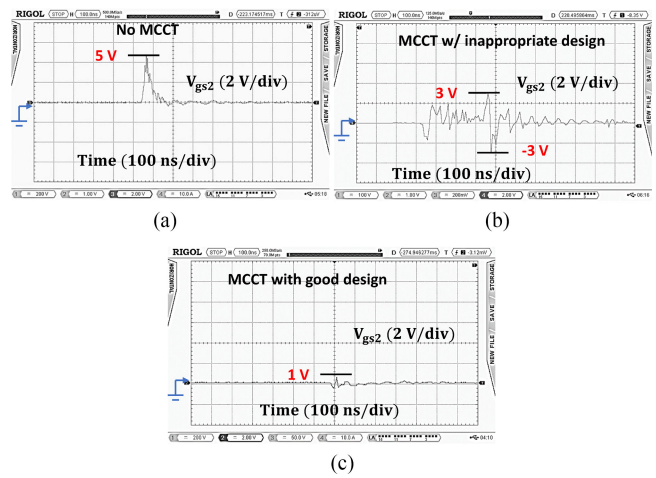


Fig. 8. Measured V_{gs} of the bottom switch when the top switch turns ON. (a) No MCCT. (b) MCCT with an inappropriate design. (c) MCCT with a good design.

Based on (17) and (18), Z_{VD} should meet the conditions (57) and (58) at frequency $10/t_{sw}$

$$\left|Z_{VD}\right| \gg \left|\frac{Z_{Q1}}{\frac{Z_3 Z_{Q1}}{Z_2+Z_3}g_{mQ1}-1}\right| \tag{57}$$

$$\left|Z_{VD}\right| \gg \left|\frac{V_{ds}}{g_{mQ1}V_{thQ1}}\right|. \tag{58}$$

The induced gate voltage of a bottom switch during the turn-ON transients of the top switch in a phase-leg configuration is shown in Fig. 8(a) under 100 V/3 A test condition (the full power tests will be conducted in Section V). Fig. 8(b) shows a case when the MCCT does not meet (57) and (58). The cancellation is not good. Fig. 8(c) shows the case when MCCT meets (57) and (58). The induced voltage is greatly canceled.

The value of C_1–C_4 must be selected based on (57) and (58) to achieve good cancellation.

C. Design of the VIC

To achieve the function of VIC, Q_2 must operate in the saturation region. Namely

$$V_{dsQ2} > V_{gsQ2} - V_{thQ2} \tag{59}$$

where V_{dsQ2}, V_{gsQ2}, and V_{thQ2} are the drain to source voltage, gate to source voltage, and the threshold voltage of Q_2, respectively. When Q_2 conducts currents, the drain to source voltage is

$$V_{dsQ2} = V_{cc} - i_{dQ2}\,(R_g//R_{\mathrm{inj}} + R_s)\,. \tag{60}$$

Substituting (24), (25), and (57) into (58), the saturation condition can be calculated as

$$V_{VS\mathrm{Max}} < \frac{V_{cc}\,(1+g_m R_s)}{g_m\,(R_g//R_{\mathrm{inj}}+R_s)+1} + V_{thQ2} \tag{61}$$

where $V_{VS\mathrm{Max}}$ is the maximum output voltage of VSC and it is

$$V_{VS\mathrm{Max}} = \frac{Z_4}{Z_{VD}}\,(V_{ds} - V_{Q1}) + V_{Q1} \tag{62}$$

where V_{Q1} is given in (19). The design should satisfy (61) for Q_2 to operate in the saturation region. At the same time, R_s should be kept small, so it will not limit the amplitude of i_{inj}.

D. Power Loss Discussion

During the MCCT operation, the extra power losses can be generated in both VSC and VIC. In VSC, the power loss is due to the charging and discharging of capacitors C_1–C_5. The total energy loss due to the charging and discharging of C_1–C_5 in one switching period is given by

$$E_{\text{VSC}} = C_{\text{eq}}\, V_{\text{DC}}^2 \tag{63}$$

where C_{eq} is the equivalent capacitance of C_1–C_5 and V_{DC} is the phase-leg's DC-link voltage. For a good design, C_{eq} should be much smaller than the output capacitance of the SiC MOSFET. Based on the design in this article, the energy loss due to the charge and discharge of $C_1 - C_5$ is 2.5 μJ each cycle. The switching energy loss for each switching cycle of the SiC MOSFET is 1.31 mJ (see Fig. 19). $C_1 - C_5$, therefore, contributes to less than 0.2% of the total switching power loss.

The power loss of the VIC is generated when there is current flowing through R_{inj}, R_s, and Q_2. When SiC MOSFET's V_{ds} is high, Q_2 conducts the current and the VIC generates the dc power loss. When SiC MOSFET's V_{ds} is low, Q_2 turns OFF and VIC does not generate power loss. Because of this, the power loss is a function of the duty cycle of the phase leg. On the other hand, the power loss on R_g due to i_{gd} is eliminated because i_{inj} cancels i_{gd}. Because of VIC's low switching current and voltage, the Q_2's switching power loss can be ignored. Because of this, the power loss is mostly from the dc power loss when Q_2 conducts currents. If the duty cycle of the phase leg is D, the power loss P_{VIC} is

$$P_{\text{VIC}} = (1-D)\left(\frac{g_{mQ2}(V_{VS\text{Max}} - V_{thQ2})}{1 + g_{mQ2}R_s} \cdot V_{cc}\right). \tag{64}$$

If D is 0.5, V_{cc} is 15 V and V_{ds} is 500 V, the maximum P_{VIC} will be 6.4 W. Since the phase leg processes a power of 15 kW (500 V/30 A), the power loss only sacrifices 0.042% efficiency. Furthermore, it will be shown in Section V that, due to the cancellation of the Miller plateau, the switching speed of the SiC MOSFETs is greatly increased. As a result, the switching power loss with the MCCT circuit is much lower than that without the MCCT applied.

The power loss of the MCCT is mainly on R_{inj} and R_s, so R_{inj} and R_s should use power resistors. The MCCT power devices can share the heatsink with the SiC MOSFETs for heat dissipation. In this article, the MCCT is mounted on the copper plate of the printed circuit board (PCB) for heat dissipation, as shown in Fig. 14. The thermal performance will be verified in Section V-B.

V. Simulation and Experimental Verification

The simulation and experiments are carried out in a phase-leg configuration, as shown in Fig. 1. The parameters are listed in Table II.

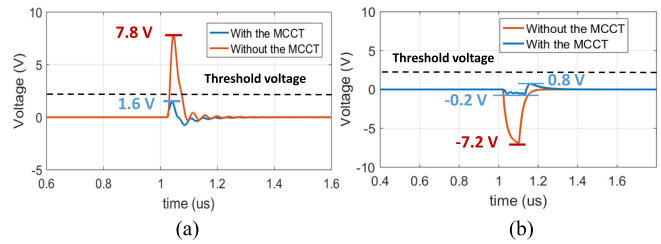


Fig. 9. Simulated V_{gs} waveforms of the bottom switch during the top switch's (a) turn-ON transient and (b) turn-OFF transient.

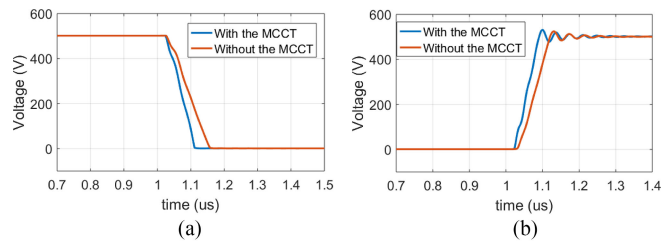


Fig. 10. Simulated V_{ds} waveforms of the bottom switch during the bottom switch's (a) turn-ON transient and (b) turn-OFF transient.

TABLE II
Parameters Used in Simulations and Experiments

Parameter	Part No.	Value/name
C_1		8.2 pF
C_2	C_{gd} of Q1+ 300pF external capacitor	400 pF
C_3	C_{gs} of Q1 + 300pF external capacitor	475 pF
C_4		1.0 nF
C_5	C_{ds} of Q1	150pF
R_{inj}		10 Ω
R_s		7.5 Ω
C_{inj}		6.8 nF
Q1	IRLMS1503	VSC MOSFET
Q2	IRLMS1503	VIC MOSFET
M1, M2	SCT3060AR	SiC MOSFETs
D1, D2	IDH20G120C5	SiC Schottky diodes
Drivers	2SC0108T2Dx	Commercial drivers

A. Simulations

The double pulse test simulations were first conducted in Ansys Simplorer. The models of the power semiconductor devices are generated with the device characterization tool of the software. Four switching transients are simulated. The gate driver voltage is $V_H = 15$ V for the turn-ON process and $V_L = 0$ V for the turn-OFF process. The simulations were conducted under a 500 V/30 A condition. The gate resistor R_g is 15 Ω. During the top switch's turn-ON and turn-OFF transients, the V_{gs} waveforms of the bottom switch are shown in Fig. 9. With the MCCT added, the positive and negative spikes are effectively suppressed by more than 85% and more than 90%. The V_{ds} waveforms during the bottom switch's turn-ON and turn-OFF transients are shown in Fig. 10. Because of the reduced Miller plateau, the turn-ON and turn-OFF speeds are increased with the MCCT. The simulation results verify the analysis in Section III.

In addition, the turn-ON and turn-OFF power losses of the SiC MOSFET are calculated based on the simulated waveforms. Because of the reduced Miller plateau, the SiC MOSFET's turn-ON

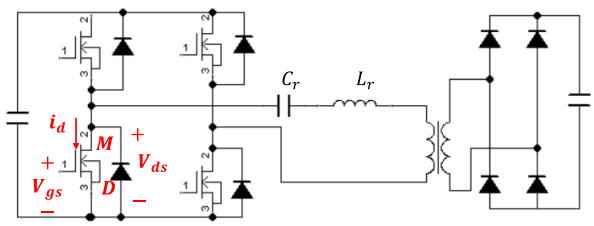
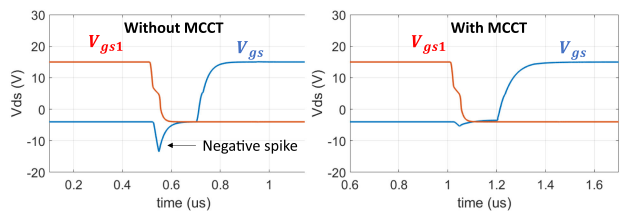
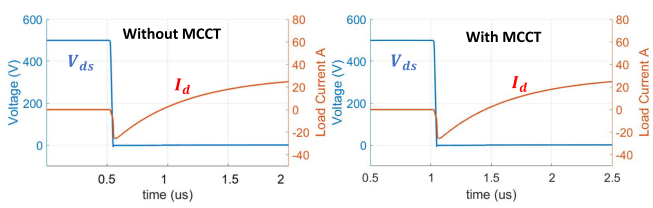


Fig. 11. Full-bridge *LLC* resonant converter used in the simulation.



(a) (b)

Fig. 12. Simulated V_{gs} waveforms for the bottom switch in a full-bridge *LLC* resonant converter under ZVS. (a) Without the MCCT. (b) With the MCCT.



(a) (b)

Fig. 13. Simulated V_{ds} and I_d waveforms for the bottom switch in a full-bridge *LLC* resonant converter under ZVS. (a) Without the MCCT. (b) With the MCCT.

and turn-OFF switching power losses are reduced by 23% and by 54% with the proposed MCCT.

Because SiC MOSFETs may operate in soft-switching mode, it is worth investigating the MCCT's impact on soft switching. The SiC MOSFET's zero voltage switching (ZVS) or zero current switching (ZCS) soft switching is usually realized with the help of body or antiparallel diodes. Because MCCT does not influence the operation of the diodes, it is expected that MCCT does not influence the soft-switching operation. Furthermore, because C_{gd} only contributes to a small part of the output capacitance of the SiC MOSFET, in case the output capacitance participates the resonant switching, the impact is also very small.

The ZVS switching of the SiC MOSFETs in an *LLC* resonant converter is simulated in Ansys Simplorer in Fig. 11 as an example. The junction capacitance and the parasitic inductance inside the package are included in the simulation.

As shown in Figs. 11 –13, during the ZVS turn-ON transition, the drain to source voltage V_{ds} of SiC MOSFET M decreases, so the Miller current is induced. Without the MCCT, the gate voltage V_{gs} of M has negative voltage spikes due to the Miller current. With the MCCT, the negative spikes are greatly suppressed. The SiC MOSFET turns ON after the antiparallel diode conducts the negative current, so M turns ON as the regular ZVS. The comparison of the simulated V_{ds} and the drain current I_d

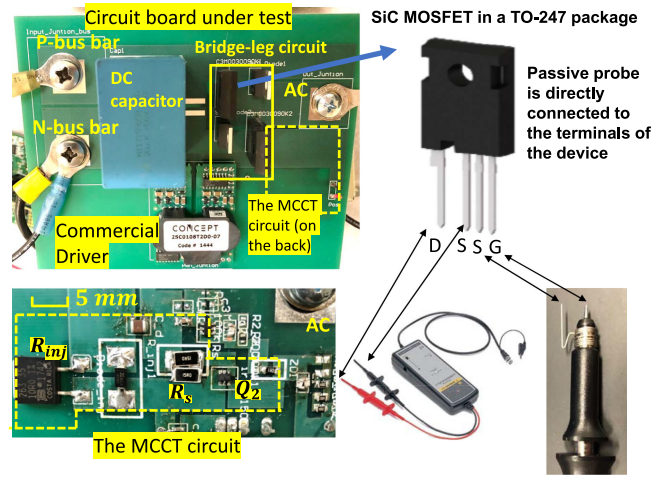


Fig. 14. Phase-leg circuit prototype and the measurement with voltage probes.

with and without MCCT in Fig. 13 validates this. The same conclusion can also be drawn for the ZCS operation.

In summary, the proposed MCCT has no negative impact on soft switching. In addition, with the proposed MCCT, the reliability of the device under soft switching is improved.

B. Experimental Verification

Two identical phase-leg prototypes, one with and the other without MCCT, are made and tested in a double pulse tester in Fig. 14. All components used in the MCCT are surface-mounted components. The footprint of the MCCT is only 5% of the phase-leg circuit's footprint. The load of the phase leg is a grounded 2.5 mH inductor. The SiC MOSFETs used in the prototype have a Kelvin gate connection. A commercial driver (2SC0108T2Dx) is employed in the experiments with the Kelvin connection to minimize the effect of the CSI. In the measurement, the probe tips are connected to the gate and Kelvin source of the SiC MOSFET package. As a result, the parasitic inductance of the probe will not generate the measurement error. The active Miller clamp function of the driver is disabled by disconnecting the Miller clamp pin. An isolated high-voltage probe is used to measure V_{ds}. Only one probe is connected to the circuit for each measurement to avoid the interference of the probe impedance [22]. In this way, both V_{gs} and V_{ds} can be accurately measured. The drain current of the device is measured with PEM Rogowski current waveform transducer. The Rogowski coil is wrapped around the drain terminal of the device package.

The prototypes are tested with 500 V dc voltage and 30 A load current. Gate resistor R_g is 15 Ω for both top and bottom switches. The measured V_{gs} of the bottom switch during the top switch switching's transients is shown in Fig. 15. The measured V_{gs} waveform when the bottom switch is OFF includes the crosstalk information between the top and bottom switches. Fig. 15(a) shows that the positive-induced gate voltage spike is reduced by 80% with the proposed MCCT. Even with 0 V OFF-state driver voltage, the gate voltage is still below the threshold voltage (2.5 V). Fig. 15(b) shows that the negative-induced gate

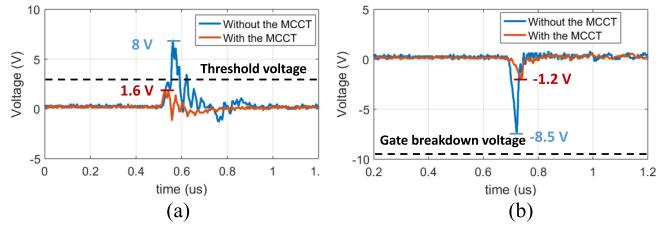


Fig. 15. Measured V_{gs} of the bottom switch without and with the MCCT during top switch's (a) turn-ON transient and (b) turn-OFF transient.

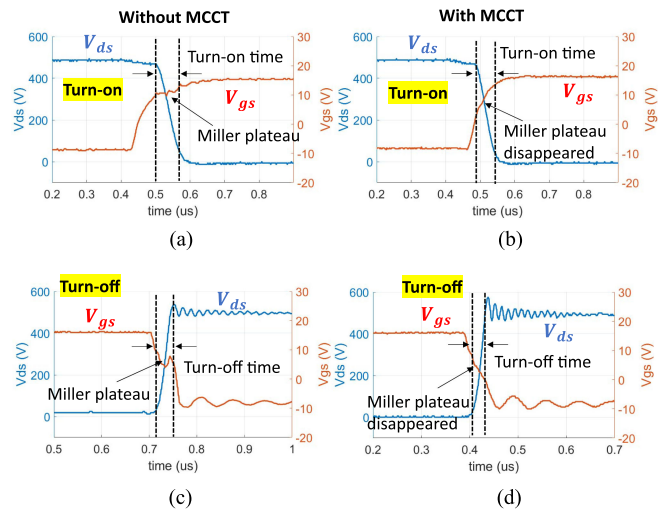


Fig. 16. Measured V_{ds} and V_{gs} waveforms of the bottom switch during the bottom switch's (a) turn-ON transient without the MCCT, (b) turn-ON transient with the MCCT, (c) turn-OFF transient without the MCCT, (d) turn-OFF transient with the MCCT.

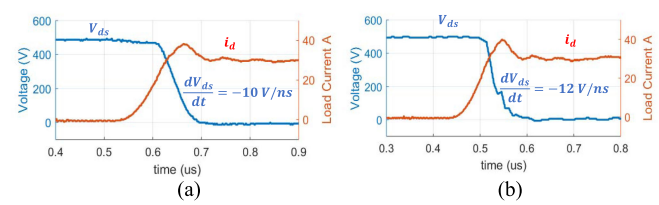


Fig. 17. Measured V_{ds} and i_d waveforms of the bottom switch during the bottom switch's turn-ON transient. (a) Without the MCCT. (b) With the MCCT.

voltage is reduced by 85% with the proposed MCCT. The excessive negative gate voltage can cause nonreversible gate–oxide breakdown. By reducing the induced gate voltage, the proposed MCCT greatly improves the reliability of SiC MOSFETs.

The measured V_{ds} and V_{gs} waveforms of the bottom switch are shown in Fig. 16. As shown in Fig. 16(b) and (d), the Miller plateau in V_{gs} waveform is canceled with the MCCT. As a result, the turn-ON and turn-OFF speeds are increased with the proposed MCCT. The measured V_{ds} and i_d waveforms of the bottom switch are shown in Figs. 17 and 18. Fig. 17 shows that the MCCT increases the turn-ON speed by 20%. Fig. 18 shows that the MCCT increases the turn-OFF speed by 50%. The switching energy loss during the turn-ON and turn-OFF transients is calculated by integrating $V_{ds}i_d$. As shown in Fig. 19, both turn-ON and turn-OFF switching energy losses are reduced with the proposed MCCT due to the increased switching speed.

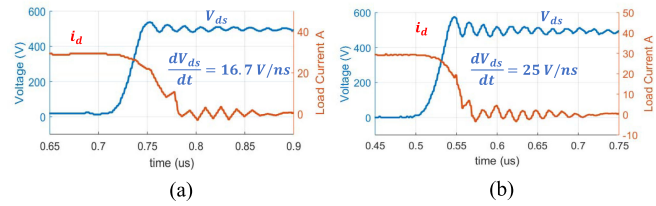


Fig. 18. Measured V_{ds} and i_d waveforms of the bottom switch during the bottom switch's turn-OFF transient. (a) Without the MCCT. (b) With the MCCT.

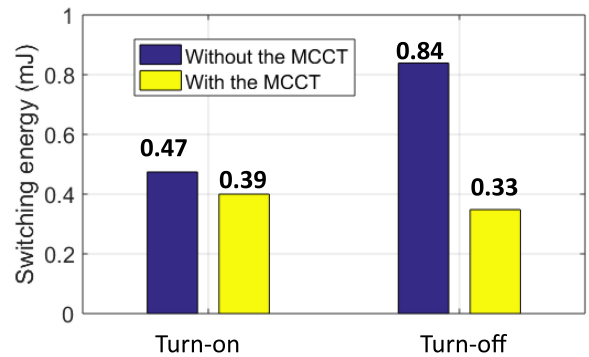


Fig. 19. Comparison of the turn-ON and turn-OFF switching energy loss for the case with and without the proposed MCCT.

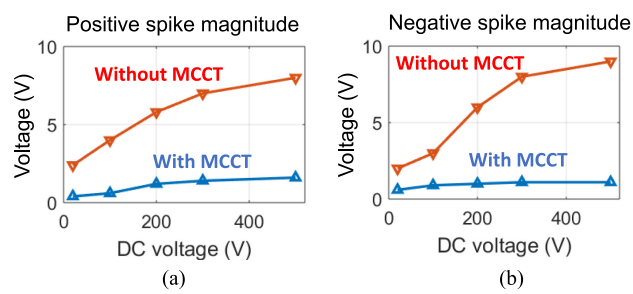


Fig. 20. Magnitudes of the induced gate voltage spikes at different DC-link voltages. (a) Positive gate voltage spikes. (b) Negative peak gate voltage spikes.

The turn-ON switching energy loss is reduced by 17%, and the turn-OFF switching energy loss is reduced by 60%. The total switching energy loss is reduced by 45% in one switching period. If the switching frequency is 100 kHz, the proposed MCCT can reduce switching power loss from 131 to 72 W. Even with the 6.4 W power loss of the MCCT, the total power loss is still reduced by 53 W (40%). With the reduced switching power loss, the SiC MOSFET with the proposed MCCT can operate at higher frequencies. The test results in Figs. 15–19 have good agreement with the analysis.

To demonstrate that the proposed MCCT can work efficiently at different voltages and currents, the induced positive and negative gate voltage spikes are measured at different dc-link voltages from 30 to 500 V while the load current is 30 A. The results are shown in Fig. 20. As shown in Fig. 20, the positive and negative gate voltage spikes increase as the dc-link voltage increases. This is because the switching speed increases when the dc voltage increases. With the proposed MCCT, the gate voltage spikes are much smaller than those without MCCT at

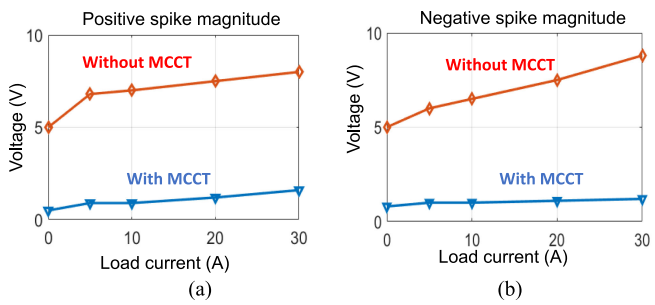


Fig. 21. Magnitudes of the induced gate voltage spikes at different load currents. (a) Positive peak gate voltage spikes. (b) Negative peak gate voltage spikes.

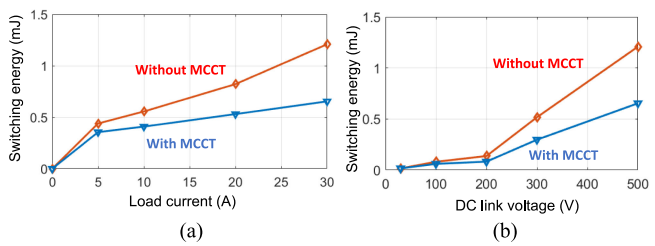


Fig. 22. Switching energy loss comparisons under different dc voltage and load currents. (a) dc voltage of 500 V and load current from 0 to 30 A. (b) Load current of 30 A and DC-link voltage from 30 to 500 V.

different dc voltages. In the next step, the gate voltage spikes are measured at different load currents from 0 to 30 A, while the dc-link voltage is 500 V. The results are shown in Fig. 21. As shown in Fig. 21, the magnitude of the induced gate voltage spikes increases as the load current increases. With the proposed MCCT, the gate voltage spikes are much smaller than those without MCCT at different currents.

The switching energy loss of the SiC MOSFET is measured under different voltages and currents. The switching energy loss for SiC MOSFET under the 500 V dc and various load currents is shown in Fig. 22(a). The switching energy loss of the SiC MOSFET under 30 A load current and various dc voltages is shown in Fig. 22(b). As shown in Fig. 22, the SiC MOSFET with the proposed MCCT has much smaller switching energy loss under different voltage and current conditions than the SiC MOSFETs without MCCT. At low dc voltage and light-load conditions, the reduced switching energy is not as significant as under the high dc voltage and high-current conditions. This is because when the DC voltages and load currents are low, the total switching energy loss is small even without the proposed MCCT. It is, therefore, concluded that the benefit of the proposed MCCT is significant under high dc voltage and high load current applications.

The prototype with the proposed MCCT is applied to a three-phase motor drive inverter, as shown in Fig. 23(a), to evaluate its performance under continuous operations. The three-phase motor drive is driven by an sinusoidal pulse width modulation (SPWM) control signal. The OFF-state voltage of the driver is −8 V to avoid shoot through. The output voltage of the phase leg is shown in Fig. 23(b). The temperature of the MCCT circuit is measured with a thermal camera. Fig. 24 shows that the highest

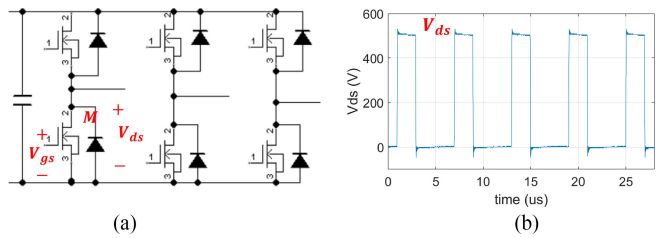


Fig. 23. Testing the MCCT in a three-phase motor drive under continuous operation. (a) Three-phase motor drive topology. (b) V_{ds} waveform.

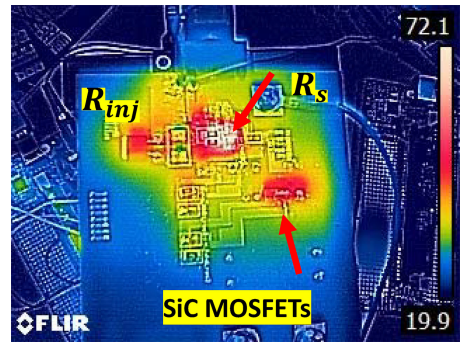


Fig. 24. Temperature of the MCCT during continuous operation.

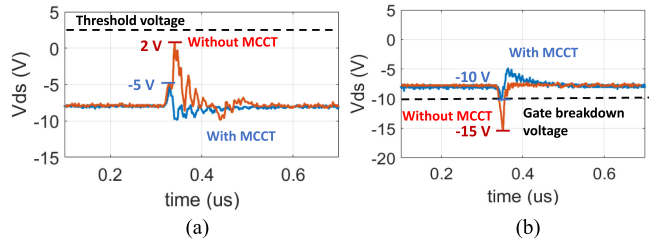


Fig. 25. Measured V_{gs} of the bottom switch during the top switch switching transients under continuous operation. (a) Top switch turn-ON. (b) Top switch turn-OFF.

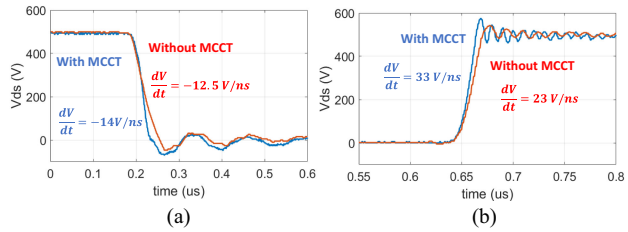


Fig. 26. Measured V_{ds} during switching transients under continuous operation. (a) Turn-ON transient. (b) Turn-OFF transient.

temperature of the MCCT under continuous operation is less than 80 °C, so there are no thermal concerns.

Figs. 25 and 26 show the measured induced gate voltage and the drain to source voltage waveforms of the bottom switch under the continuous operation. The temperature of the MCCT in this measurement is 72 °C. Under continuous operation, the proposed MCCT reduces the positive gate voltage spikes by 70% and negative spikes by 71.4%. The turn-ON speed is increased by 12%, and the turn-OFF speed is increased by 60% with the MCCT.

VI. Conclusion

This article proposed an MCCT for SiC MOSFETs in a phase-leg configuration. The proposed MCCT cancels the effects of Miller capacitance by injecting a mirror cancellation current. The nonlinearity of the Miller capacitance is compensated with a two-stage gain solution. The design technique for the proposed MCCT is also discussed. It has been validated with both simulations and experiments that the proposed MCCT can effectively reduce crosstalk, eliminate Miller plateau, increase switching speed, reduce switching power loss, and may improve SiC MOSFET's reliability. The proposed MCCT can easily work with most of the commercial drivers.

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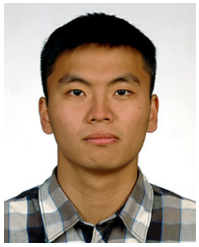

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